~~18. (New) A liquid crystal display~~ comprising:

a liquid crystal panel;

a decoder adapted to convert an inputted image signal into an image signal adaptable to said liquid crystal panel,

~~wherein~~ said decoder is provided with a memory controller according to Claim 1.

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REMARKS

This application has been reviewed in light of the Office Action dated May 22, 2002. Claims 17 and 18 are presented for examination and have been added to provide Applicants with a more complete scope of protection. Claims13-16 have been canceled, without prejudice or disclaimer of the subject matter presented therein. Claim 17 is in independent form. Favorable reconsideration is requested.

Applicants noticed that one of the references cited on the PTO-1449 form accompanying the Information Disclosure Statement submitted on July 1, 1999 was not initialed by the Examiner, although all the other references were initialed (copy attached). Applicants respectfully request return of a copy of that PTO-1449 with all the cited references initialed, including JP 4-259079.

The Office Action rejected Claims 13-16 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,745,485 (Iwasaki) in view of U.S. Patent No. 4,864,402 (Ebihara et al.), and further in view of U.S. Patent No. 5,794,016 (Kelleher). Claims 13 and 15 also were objected to for certain informalities. Cancellation of Claims 13-16 renders their

rejections moot. Applicants submit that independent Claim 17 is patentable over Iwasaki, Ebihara et al., and Kelleher for at least the following reasons.

The aspect of the present invention set forth in Claim 17 is directed to a memory controller that includes a converter section, a first FIFO section, a frame memory section, a second FIFO section, and a control unit. The converter section performs serial/parallel conversion of image data of a bit width as inputted into image data of ax2n bit width. The first FIFO temporarily stores the image data of ax2n bit width. The frame memory section stores image data of one frame, based on a signal from the first FIFO, and the second FIFO section temporarily stores image data read out from the frame memory section. The control unit performs a control process, such that image data is read out from the first FIFO section, written into the frame memory section, and read out from the frame memory section at a rate that is half of a rate at which the image data is inputted into the first FIFO section. The first FIFO section is of a size suitable for storing image data inputted during a period that equals a sum of a period for reading image data from the frame memory unit a plurality of times and a period necessary for command of the frame memory unit.

Iwasaki, as understood by Applicants, relates to a picture display device that alternately selects an address output of a write address counter and an address output of read address counters. Ebihara et al., as understood by Applicants, relates to a video memory. Kelleher, as understood by Applicant, relates to a parallel-processor graphics architecture.

Applicant submits that a combination of Iwasaki, Ebihara et al., and Kelleher, assuming such combination would even be permissible, would fail to teach or suggest a memory controller that includes "a converter section adapted to perform serial/parallel conversion of

image data of an inputted bit width into image data of ax2n bit width," and "a first FIFO (first-in-first-out) section adapted to temporarily store the image data of ax2n bit width," and "a frame memory section adapted to store image data of one frame, based on a signal from said first FIFO" and "a second FIFO section adapted to temporarily store image data read out from said frame memory section," and "a control unit adapted to perform a control process, such that image data is read out from said first FIFO section, written into said frame memory section, and read out from said frame memory section at a rate that is half of a rate at which the image data is inputted into said first FIFO section," wherein "said first FIFO section is of a size suitable for storing image data inputted during a period that equals a sum of a period of reading image data from said frame memory unit a plurality of times and a period necessary for command of said frame memory unit," as recited in Claim 17.

Apparently, according to Fig. 1 of Iwasaki, LATCH 6 is controlled by a latch signal from LATCH 3. In contrast, the second FIFO section of Claim 17, which may be considered to correspond to the LATCH 6 of Iwasaki, is controlled by a signal from the frame memory. More specifically, Applicants submit that Iwasaki fails to teach or suggest that a second FIFO is controlled by a signal from a frame memory which, in turn, is controlled by a signal from a first FIFO. Neither Ebihara et al. nor Kelleher are believed to remedy the deficiencies of Iwasaki.

Accordingly, Applicants submit that Claim 17 is patentable over Iwasaki, Ebihara et al., and Kelleher, considered separately or in combination. Claim 18 depends from Claim 17 and, therefore, is submitted to be patentable for at least the same reasons. Since a dependent claim is also deemed to define an additional aspect of the invention, individual

consideration of the patentability of Claim 18 on its own merits is respectfully requested.

This Amendment After Final Action is believed clearly to place this application in condition for allowance and, therefore, its entry is believed proper under 37 C.F.R. § 1.116. Accordingly, entry of this Amendment, as an earnest effort to advance prosecution and reduce the number of issues, is respectfully requested. Should the Examiner believe that issues remain outstanding, it is respectfully requested that the Examiner contact Applicants' undersigned attorney in an effort to resolve such issues and advance the case to issue.

In view of the foregoing amendments and remarks, Applicants respectfully request favorable reconsideration and early passage to issue of the present application.

Applicants' undersigned attorney may be reached in our New York Office by telephone at (212) 218-2100. All correspondence should continue to be directed to our address listed below.

Respectfully submitted,

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